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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/550,741
Filing Date: September 22, 2005
Appellant(s): SURDEANU ET AL.

Robert Crawford
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 10, 2010 appealing from the Office action mailed December 11, 2009.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application: 6-14 and 17-24.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

6,667,525	Rhee et al.	12-2003
2001/0039107	Suguro	11-2001
6,399,515	Tao et al.	06-2002
6,222,251	Holloway	04-2001
6,160,300	Gardner et al.	12-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 7, 10-14, 17 and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,667,525, granted to "**Rhee**," in view of U.S. PGPUB 2001/0039107, granted to "**Suguro**," U.S. Patent 6,399,515, granted to "**Tao**."

Claims 6, 7 and 17: Rhee discloses an MIS type semiconductor device, Fig. 3, comprising:

a semiconductor substrate (21),

a gate electrode (23 and 24) formed on a gate insulating film (22) and formed of gate material,

wherein the gate electrode comprises:

a first layer of activated crystalline gate material (23) having a first side oriented towards the substrate and in contact with the gate insulating film, a second side oriented away from the substrate and a grain size, and

a second layer of gate material (24) in contact with the first layer of activated crystalline gate material at the second side of the first layer of activated crystalline gate material, the second layer of gate material having a grain size,

wherein the grain size of the first layer of activated crystalline gate material is smaller than the grain size of the second layer of gate material (column 5, lines 5-52).

Rhee appears not to explicitly disclose the grain size of the second layer of gate material is at least twice as large as the grain size of the first layer of activated crystalline gate material.

Suguro, however, discloses a gate electrode with a second layer (3') having a grain size at least twice as large as the grain size of a first layer (3) to reduce the variations in threshold voltage (Fig. 3; paragraphs [0081]-[0096]).

To reduce the variations in threshold voltage therefore it would have been obvious to modify Rhee to have made the grain size of the second layer of gate material is at least twice as large as the grain size of the first layer of activated crystalline gate material.

Rhee also appears not to explicitly disclose the first layer of activated crystalline gate material having a doping level of 10^{19} ions/cm^3 (claim 6), 10^{20} ions/cm^3 (claim 7), $5x10^{20}$ ions/cm^3 (claim 17) or higher.

Tao, however, discloses and motivates a gate electrode doped to a level greater than about 10^{20} dopant atoms per cubic centimeter in order to assure optimal conductivity (column 9, lines 14-37).

To assure optimal conductivity therefore it would have been obvious to modify Rhee so the first layer of activated crystalline gate material has a doping level greater than 10^{19} ions/cm^3. In the case where the claimed ranges overlap or lie inside ranges disclosed by the prior art a *prima facie* case of obviousness exists (M.P.E.P. § 2144.05).

Claim 10: Rhee discloses the second layer of gate material consists of polycrystalline gate material (column 5, lines 5-10).

Claim 11: Suguro discloses the grain size of the second layer is more than 30 nm (paragraph [0094]). In the case where the claimed ranges overlap or lie inside ranges disclosed by the prior art a *prima facie* case of obviousness exists (M.P.E.P. § 2144.05). It would therefore have been obvious to have made the grain size in the second layer below about 40 nm.

Claims 12, 20 and 21: Suguro discloses the first layer is crystalline and has grains below 10 nm. In the case where the claimed ranges overlap or lie inside ranges disclosed by the prior art a *prima facie* case of obviousness exists (M.P.E.P. § 2144.05). It would therefore have been obvious to have made the first layer have grains below 5 nm. Suguro also discloses the grain size in the second layer is below about 30 nm (paragraph [0094]). Suguro therefore disclose the grain size of the second layer of gate material is about six times as large as the grain size of the first layer of activated crystalline gate material.

Claim 13: Rhee discloses a gate insulator (22) is provided between the semiconductor substrate and the gate electrode (Fig. 3; column 5, lines 26-27).

Claim 14: Gardner et al. teach the device is a transistor (column 5, lines 5-6).

Claim 22: The recitation "the grain size of the first layer of activated crystalline gate material reduces gaps between the first layer of activated crystalline gate material and the gate insulating film" has been considered and determined to be functional language, making the claim scope not distinguish over a layer of activated crystalline gate material capable of having grain size to reduce gaps between a layer of activated crystalline gate material and a gate insulting film. The claim recitations do not require the grain size of the first layer of activated crystalline gate material reduces gaps between the first layer of activated crystalline gate material and the gate insulating film to be part of the elements limiting the claim scope. See MPEP § 2114, and precedents cited therein.

Claim 23: Rhee discloses the first layer of activated crystalline gate material is silicon (column 5, lines 5-10).

Claim 24: Rhee discloses an MIS type semiconductor device, Fig. 3, comprising:

a semiconductor substrate (21);

a gate insulating film (22); and

a gate electrode (23 and 24) formed on the gate insulating film, the gate electrode including:

a first layer of activated crystalline gate material (23) having a first side oriented towards the substrate and in contact with the gate insulating film, a second side oriented away from the substrate and a grain size of less than about 5 nm, and

a second layer of gate material (24) in contact with the first layer of activated crystalline gate material at the second side of the first layer of activated crystalline gate material, the second layer of gate material having a grain size of less than about 40 nm,

wherein the grain size of the first layer of activated crystalline gate material is smaller than the grain size of the second layer of gate material (column 5, lines 5-52).

Rhee appears not to explicitly disclose the first layer of activated crystalline gate material has a grain size of less than about 5 nm and the second layer of gate material has a grain size of less than about 40 nm.

Suguro, however, discloses a gate electrode with a first layer (3) with a grain size of 10 nm or less and a second layer (3') having a grain size of more than 30nm to reduce the variations in threshold voltage (Fig. 3; paragraphs [0081]-[0096]).

To reduce the variations in threshold voltage therefore it would have been obvious to modify Rhee to have made the first layer of activated crystalline gate material have a grain size of less than about 5 nm and the second layer of gate material have a grain size of less than about 40 nm. In the case where the claimed ranges overlap or lie inside ranges disclosed by the prior art a *prima facie* case of obviousness exists (M.P.E.P. § 2144.05).

Rhee also appears not to explicitly disclose the first layer of activated crystalline gate material having a doping level of 10^{19} ions/cm^3.

Tao, however, discloses and motivates a gate electrode doped to a level greater than about 10^{20} dopant atoms per cubic centimeter in order to assure optimal conductivity (column 9, lines 14-37).

To assure optimal conductivity therefore it would have been obvious to modify Rhee so the first layer of activated crystalline gate material has a doping level greater than 10^{19} ions/cm^3. In the case where the claimed ranges overlap or lie inside ranges disclosed by the prior art a *prima facie* case of obviousness exists (M.P.E.P. § 2144.05).

Claims 8, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee in view of Suguro in view of Tao as applied to claims 6, 7, 10-14, 17 and 20-24 above, and further in view of U.S. Patent 6,222,251, granted to "**Holloway**."

Claims 8, 18 and 19: Rhee in view of Tao discloses all the limitations of claim of claim 6. Rhee in view of Tao appears not to explicitly disclose the doping implant in the activated gate material has an abruptness of about 2nm or more (claim 8); about 1.5nm (claim 18) or more; or about 1nm (claim 19).

Holloway discloses the doping profile across a gate electrode is a resulting-affecting parameter. Holloway discloses having a doping profile across a gate electrode from an upper surface to a gate oxide boundary affects the depletion region of the gate (column 5, line 30—column 6, line 8) and further discloses that different applications desires different depletion regions (column 1, line 56 – column 2, line 3).

Since Holloway discloses the doping profile across a gate electrode is a result-affecting parameter, therefore it would have been obvious to optimize the doping profile of a gate, such as the abruptness of the doping profile (see M.P.E.P. § 2144.05).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee in view of Suguro in view of Tao as applied to claims 6, 7, 10-14, 17 and 20-24 above, and further in view of U.S. Patent 6,160,300, granted to "**Gardner**."

Claim 9: Rhee in view of Tao discloses all the limitations of claim of claim 6 and Rhee further discloses the second layer of gate material consists of polycrystalline gate material (column 5, lines 5-10). Rhee in view of Tao appears not to explicitly disclose the second layer of gate material consists of amorphous gate material.

Gardner, however, discloses polysilicon and amorphous silicon are suitable materials for an upper layer of a gate electrode (column 7, lines 21-32). The selection of a known material based on its suitability for its intended purpose is obvious (see, for example, MPEP § 2144.07, and precedents cited therein).

Because polysilicon and amorphous silicon are art-recognized suitable materials for an upper layer of a gate electrode, therefore, it would have been obvious to modify Rhee to have made the second layer of gate material from amorphous gate material.

(10) Response to Argument

A. The Rejection of Claims 6-7, 11-14, 17 and 20-24

Appellant contends the combination of the grain sizes of a metal gate electrode disclosed in Suguro and the semiconductor gate layers of Rhee, that metallic and polysilicon materials exhibit different semiconductor properties that cannot be combined as proposed without extensive modification. Appellant further contends since the proposed combination lacks any supporting evidence, and further does not provide a clearly-articulated reason (or explanation as to how Rhee could or would operate as modified), the § 103(a) rejection is improper for lack of motivation.

Examiner notes that the proposed combination was to modify the grain sizes of the gate layers 23 and 24 of Rhee to have the grain sizes discloses by Suguro. Rhee discloses the lower gate layer 23 has smaller a grain size than the upper gate layer 24 (Fig. 3; column 5, lines 5-10), but does not seem to explicitly disclose by how much smaller or the actual grain size of each layer. Suguro discloses the lower gate electrode 3 has a grain size of 10 nm or less and an upper gate electrode of 30 nm or more (Fig. 3; paragraphs [0082] and [0094]). Since Rhee discloses that the upper gate layer 24 (second layer in claims 6 and 24) is greater than the lower gate layer 23 (first layer in claims 6 and 24), one of ordinary skill in the art would have been able to modify Rhee with the disclosure of Suguro without undue experimentation to have the grain size of layer 24 at least twice as large as the grain size of layer 23 or to have the grain size of layer 23 less than about 5 nm and the grain size of layer 24 less than about 40 nm.

It is known in the art to modify the properties of the gate electrode, such as the grain size of the gate electrode, to optimize the performance of a device, such as by reducing variations threshold voltage. For example, Rhee discloses threshold voltage fluctuates when dopants get into the gate oxide (column 2, lines 5-13). To solve the dopant penetrations issue, a poly-SiGe layer is used for the gate (column 2, lines 24-31). To increase the conductivity of the gate with poly-SiGe, a poly-Si layer is formed on top of the poly-SiGe (column 2, lines 43-49). Rhee then discloses to prevent Ge from diffusing from the poly-SiGe layer to the poly-Si layer, the grain boundary between the layer shot not be formed continuously (column 5, lines 5-22). Therefore Rhee discloses grain sizes of the gate layers have a correlation with the threshold voltage. One of ordinary skill in the art would have been motivated to modify the grain sizes of Rhee to gain the advantages disclosed in Suguro. Combining the disclosure of Sugruo with Rhee will not change the operation of Rhee because Rhee discloses the need to decrease the fluctuation of the threshold voltage and to have a difference in the grain sizes.

Examiner further notes that although Rhee does not explicitly disclose the grain sizes of gate layers 23 and 24, Fig. 3 shows the grain boundaries of the layers. From Fig. 3, it can be seen that the grain size of the upper gate layer 24 is at least twice as large as the grain size of the lower gate layer 23.

Appellant contends the rejection does not provide any support or reasoning for the conclusion that grain size of polysilicon will exhibit semiconductor properties expected as grain sizes used in connection with metallic compounds.

Examiner notes that Rhee discloses the lower gate layer 23 has smaller a grain size than the upper gate layer 24 (Fig. 3; column 5, lines 5-10). It is also well known in the art to modify semiconductive gate electrodes to obtain desired threshold voltages. With the disclosure of Suguro, it would have been obvious to one of ordinary skill in the art to modify Rhee with a reasonable expectation of success.

Appellant contends replacing polysilicon gate electrodes with metalized gate electrodes introduces several problems.

Examiner notes that the combination of Rhee and Suguro used in the rejection did not replace the semiconductive electrode layer of Rhee with metal electrode layers of Suguro. The combination modified the semiconductive electrode layers of Rhee to have the grain sizes disclosed by Suguro.

Appellant contends an explanation as to why the metal grain size of Suguro would be view as relevant to activated silicon gate material.

Examiner notes Suguro discloses a gate electrode with a second layer (3') having a grain size at least twice as large as the grain size of a first layer (3) to reduce the variations in threshold voltage (Fig. 3; paragraphs [0081]-[0096]). It is also well known in the art to modify semiconductive gate electrodes to obtain desired threshold voltages. With the disclosure of Suguro, one of ordinary skill in the art would be motivated to modify Rhee with a reasonable expectation of success.

Appellant contends Suguro teaches away from replacing the polysilicon-based grains with metal-based grains in paragraph [0078].

Examiner notes that paragraph [0078] of Suguro does not disclose disadvantages of replacing polysilicon-based grains with metal-based grains. Paragraph [0078] discloses a problem with metal gate electrodes in MOS transistor. Suguro in paragraph [0079] discloses that they are solving the problem of metal gate electrodes in MOS transistors.

Appellant contends Examiner did not consider Suguro as a whole, instead focused on individual elements.

Examiner notes that Suguro was considered as a whole, but only a certain part of Suguro was used for the rejection. Suguro discloses a gate electrode with a second layer (3') having a grain size at least twice as large as the grain size of a first layer (3) to reduce the variations in threshold voltage (Fig. 3; paragraphs [0081]-[0096]). It is also well known in the art to modify semiconductive gate electrodes to obtain desired threshold voltages. With the disclosure of Suguro, one of ordinary skill in the art would be motivated to modify Rhee with a reasonable expectation of success.

B. The Rejection of Claims 8 and 18-19

Appellant contends Examiner improperly asserts that the abruptness of doping concentration is simply a recognized parameter despite no mention therefore in any of the references.

Examiner notes that Holloway was provided for the disclosure of abruptness.

Appellant contends none of the cited references has been shown to teach the abruptness of the doping profiles because the teaching are relatively general and relate

simply to the overall doping level, such as optimization for conductivity. Appellant points to column 1, lines 38-41.

Examiner notes that Holloway discloses the doping profile across a gate electrode is a resulting-affecting parameter. Holloway discloses having a doping profile across a gate electrode from an upper surface to a gate oxide boundary affects the depletion region of the gate (column 5, line 30—column 6, line 8) and further discloses that different applications desires different depletion regions (column 1, line 56 – column 2, line 3).

Appellant contends none of the cited references consider problems of the penetration of dopants from the gate into the gate insulation and channel regions during implantation and dopant activation, which results in decreased performance, as discussed throughout Appellant's specification.

Examiner notes that on page 8, lines 24-28 of the Appellant's Appeal Brief, Appellant discuses how Rhee and Suguro both disclose problems with dopant penetration. Examiner further notes that the cited disclosures of Rhee and Suguro by Appellant are in the background section, and Rhee and Suguro further disclose that those are problems being solved.

Appellant contends Holloway fails to fix the deficiencies of Rhee and Suguro in Section A above.

Examiner notes that Rhee and Suguro are discussed above.

C. The Rejection of Claim 9

Appellant contends Rhee teaches away from an amorphous upper gate. Appellant cites Rhee at column 4, line 50 – column 5, line 22, contending that Rhee discloses restraining the diffusion of Ge through the grain boundary from the lower layer 23 to the upper layer 24 by giving the lower layer 23 a columnar crystalline structure and the upper layer 24 random crystalline structure.

Examiner notes that the cited disclosure of Rhee by Appellant is the problem in which Rhee is trying to solve. Rhee at column 4, line 59 – column 5, line 4 is discussing a conventional gate structure in which the upper and lower layers of the gate have a continuous grain boundary, the continuous grain boundary allows Ge to easily diffuse from the lower layer to the upper layer. Then at column 5, lines 5-22, Rhee discloses how they solve the problem. Rhee solves the diffusion problem by having the grain boundary of the lower layer not formed continuously with the grain boundary of the upper layer. Since amorphous semiconductor material does not have a regular crystal structure, the boundary between the upper layer and the lower layer will not have a continuous grain boundary and therefore Ge will not be able to diffuse from the lower layer to the upper layer.

Examiner further notes that an amorphous gate material does not have a grain size. Grains are a property of crystalline material not amorphous. Therefore claim 9 has to be an intermediate step in the manufacturing of the parent claim 6 because the second layer cannot be an amorphous material and have a grain size at the same time.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/J. L./

Examiner, Art Unit 2815

/KENNETH A PARKER/

Supervisory Patent Examiner, Art Unit 2815

Conferees:

/K. A. P./

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/Tom Thomas/